What is claimed is:

1. A method of forming a transistor, comprising:

forming a silicidation barrier on a patterned polysilicon layer;

implanting dopants to form a source/drain extension layer self-aligned to the patterned polysilicon;

forming a first silicide layer over the source/drain extension layer;

forming sidewall spacers adjacent to the patterned polysilicon;

removing a portion of the silicidation barrier from a top surface of the patterned polysilicon;

forming a second silicide layer self-aligned to the sidewall spacers; and

forming a third silicide layer on a top surface of the patterned polysilicon.

2. The method of Claim 1 wherein the second silicide layer and the third silicide layer are formed concurrently.

3. The method of Claim 1, wherein forming a silicidation barrier comprises nitridizing the patterned polysilicon layer.

4. The method of Claim 1, wherein forming the silicidation barrier comprises forming a silicon nitride layer on a top surface of the patterned polysilicon, and on at least one sidewall of the patterned polysilicon.

5. The method of Claim 1, wherein the silicidation barrier has a thickness sufficient to prevent silicidation of the polysilicon.

6. The method of Claim 1, further comprising depositing a layer of metal over the source/drain extension layer, wherein the metal is selected from the group consisting of titanium and cobalt.

7. The method of Claim 6, wherein further comprising depositing a layer of metal over the first silicide layer, wherein the metal is selected from the group consisting of nickel and cobalt.

8. The method of Claim 1, wherein the second and third silicide layers comprise nickel silicide.

9. The method of Claim 1, further comprising implanting dopants through the first silicide layer to form source/drains self-aligned to the sidewall spacers.

10. A method of forming a microelectronic device, comprising:

forming a patterned polysilicon layer over a dielectric layer, the dielectric layer disposed on a substrate, the patterned polysilicon having sidewalls and a top surface;

nitridizing the sidewalls and top surface of the polysilicon;

implanting first dopants into the substrate to form a source/drain extension layer;

forming a first silicide layer over the source/drain extension layer;

forming sidewall spacers adjacent to the sidewalls;

implanting second dopants through the first silicide layer into a source/drain region; and

forming a second silicide self-aligned to the sidewall spacers.

11. The method of Claim 10, further comprising thermally activating the first dopants prior to implanting the second dopant atoms.

12. The method of Claim 10 wherein the first and second silicides comprise different metals.

13. The method of Claim 10 wherein the first and second silicides comprise the same metal.

14. The method of Claim 10 wherein nitridizing the polysilicon produces a silicon nitride layer approximately 10 angstroms thick.

15. The method of Claim 10, further comprising forming an agglomeration-free silicide layer over the patterned polysilicon.

16. The method of Claim 10, further comprising removing the nitridized portion of the top surface of the gate electrode.

17. The method of Claim 10, wherein the second silicide layer is formed through the first silicide layer.

18. A microelectronic structure, comprising:

a gate electrode having sidewalls;

a silicidation barrier adjacent to the sidewalls;

a first silicide layer superjacent the gate electrode; and

a pair of source/drain terminals self-aligned to the gate electrode;

wherein the source/drain terminals comprise a first implanted region, a second silicide layer; a second implanted regions and a third silicide layer.

19. The microelectronic structure of Claim 18, wherein the second silicide layer is contained within the first implanted region.

20. The microelectronic structure of Claim 18, wherein the third silicide layer is thicker than the first implanted region.